WBS 3.2 — Data Acquisition

Paris Sphicas, *CERN/MIT*
US_CMS L2 DAQ manager

DOE/NSF Review
May 19, 1998

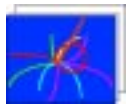
Outline

DAQ System Overview
Organization
Milestones/Schedule
Evolution of US-DAQ project
Status & Progress
WBS Summary
Commitment and Resource Profiles
Concerns & Actions taken
Summary & Conclusion

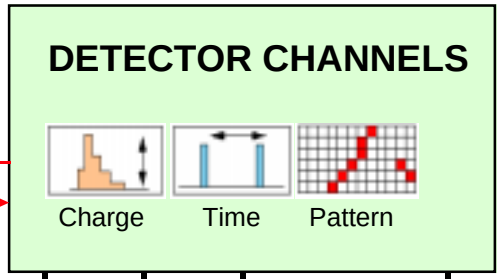
DAQ System Overview

System Overview
Overview: Architecture
Overview: CMS & Industry
US on CMS DAQ

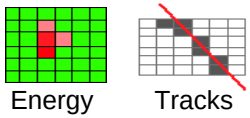
System Overview



40 MHz
COLLISION RATE



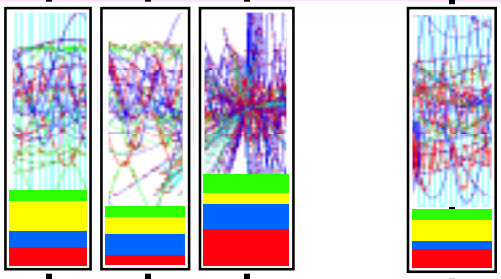
16 Million channels
3 Gigacell buffers



75 kHz

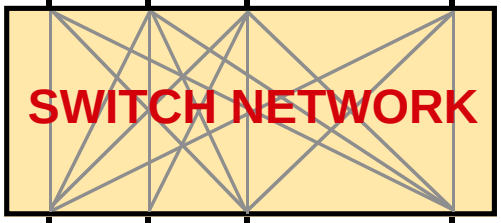
1 Megabyte EVENT DATA

1 Terabit/s
READOUT
50,000 data channels

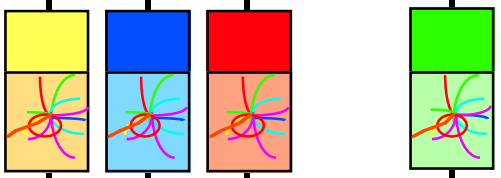


200 Gigabyte BUFFERS
~ 400 Readout memories

500 Gigabit/s



EVENT BUILDER.
A large switching network (400+400 ports) with total throughput ~ 400 Gbit/s forms the interconnection between the sources (deep buffers) and the destinations (buffers before farm CPUs). The Event Manager distributes event building commands (assigns events to destinations)

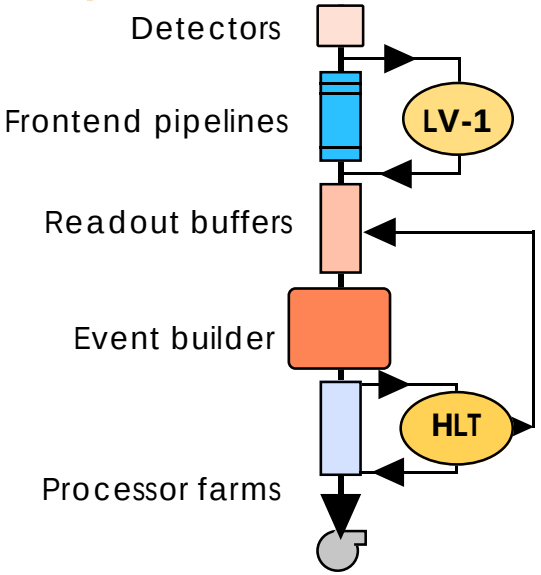


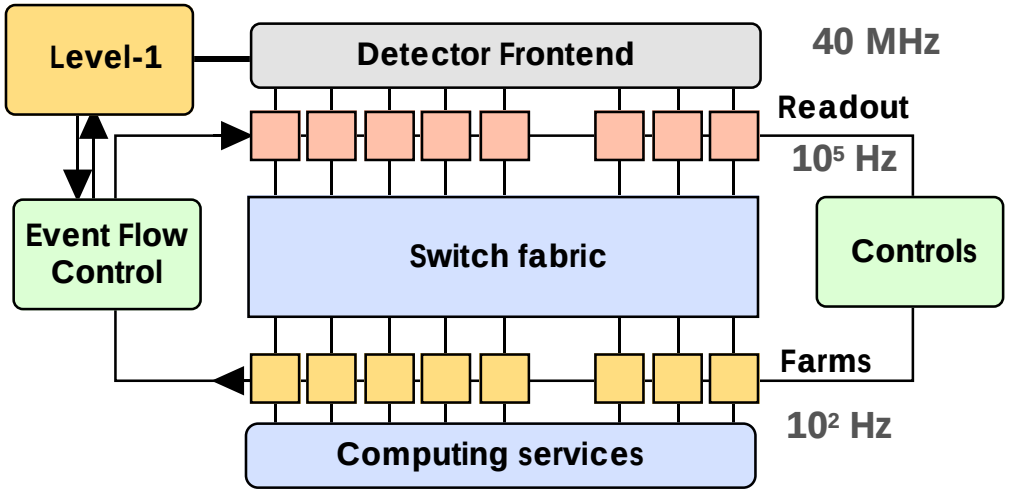
5 TeraIPS 400 CPU farms
EVENT FILTER.
A set of high performance commercial processors organized into many farms convenient for on-line and off-line applications.

100 Hz
FILTERED EVENT
Gigabit/s
SERVICE LAN

Petabyte ARCHIVE

Overview: Architecture





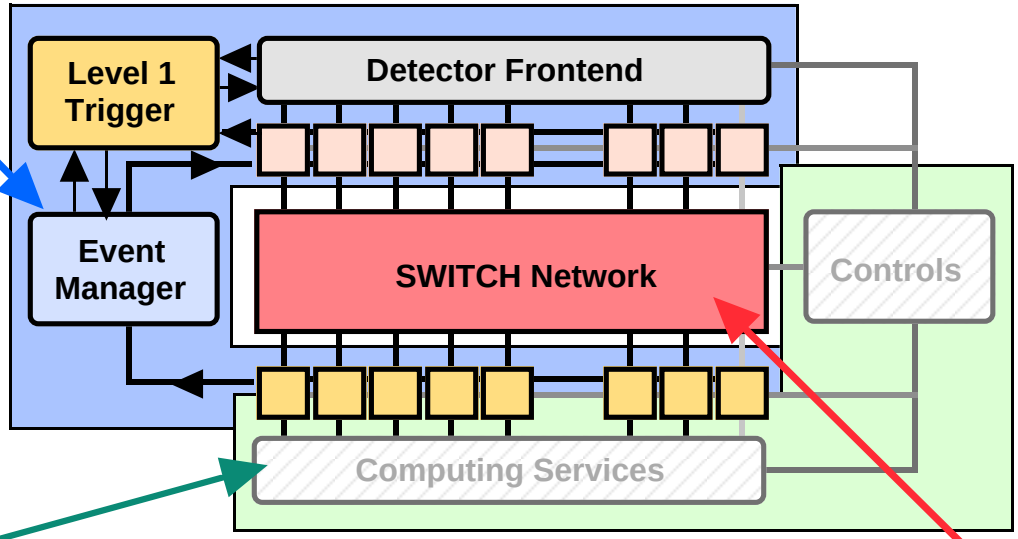
High-Level Triggers: No hardware Level-2 processor
Level-2 & Level-3 Trigger selection in CPU farm

Collision rate	**40 MHz**
Level-1 Maximum trigger rate	**75 kHz**
Average event size	**1 Mbyte**
No. of In-Out units (200-5000 byte/event)	**400**
Event builder (400+400 switch) bandwidth	**400 Gbit/s**
Event filter computing power	**5 10^6 MIPS**
Data production	**Tbyte/day**
No. of electronics boards	**10000**

Overview: CMS & Industry

CMS experiment:

Data communication technology evaluation by Integration of commercial products in experiment prototypes



Laboratory support

Slow control infrastructures
Farm organization
Generic computing services

Industry:

Data links
Switching technology

US on CMS DAQ

FNAL V. Odell CDF, D0, SDC, ...

- Engr/Tech: E. Barsotti, M. Bowden, W. Knopf, R. Kwarciany
- Phys: V. Odell, I. Gaines

MIT P. Sphicas UA1&CDF (DAQ/HLT)

- Engr & Tech: B. Wadsworth, S. Pavlon
- Phys: P. Sphicas, K. Sumorok, S. Tether, J. Tseng
- Students: P. Ngan, T. Shah, D. Vucinic

N/eastern L. Taylor L3 (Offline)

UCLA S. Erhan UA8 & HERA-B (DAQ)

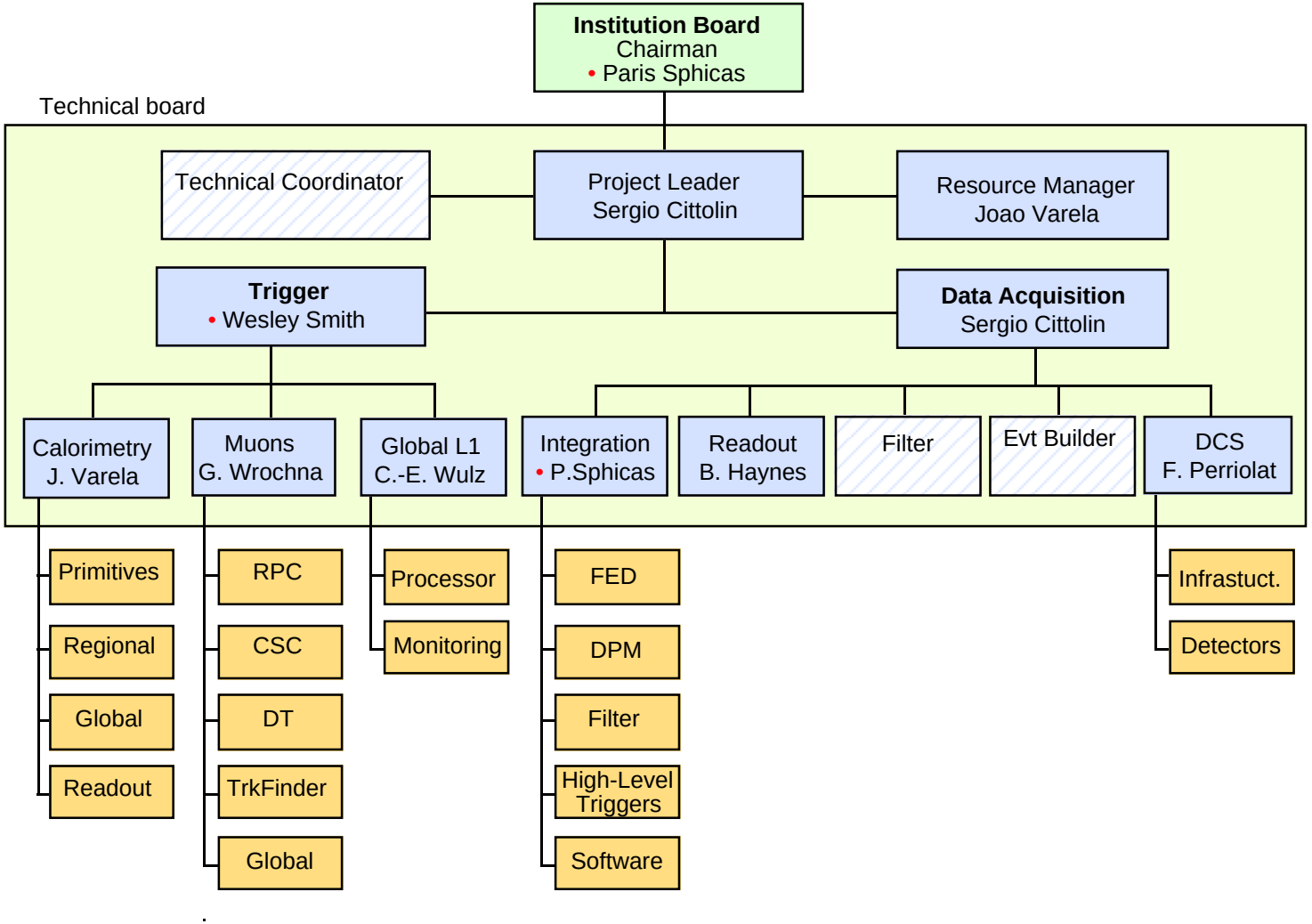
UCSD J.Branson GEM (DAQ); L3 (Offline)

- Engr & Tech: M. Mojaver, A. White, J. Armstrong
- Phys: J. Branson, H. Kobrak, H. Paar
- Students: I. Fisk

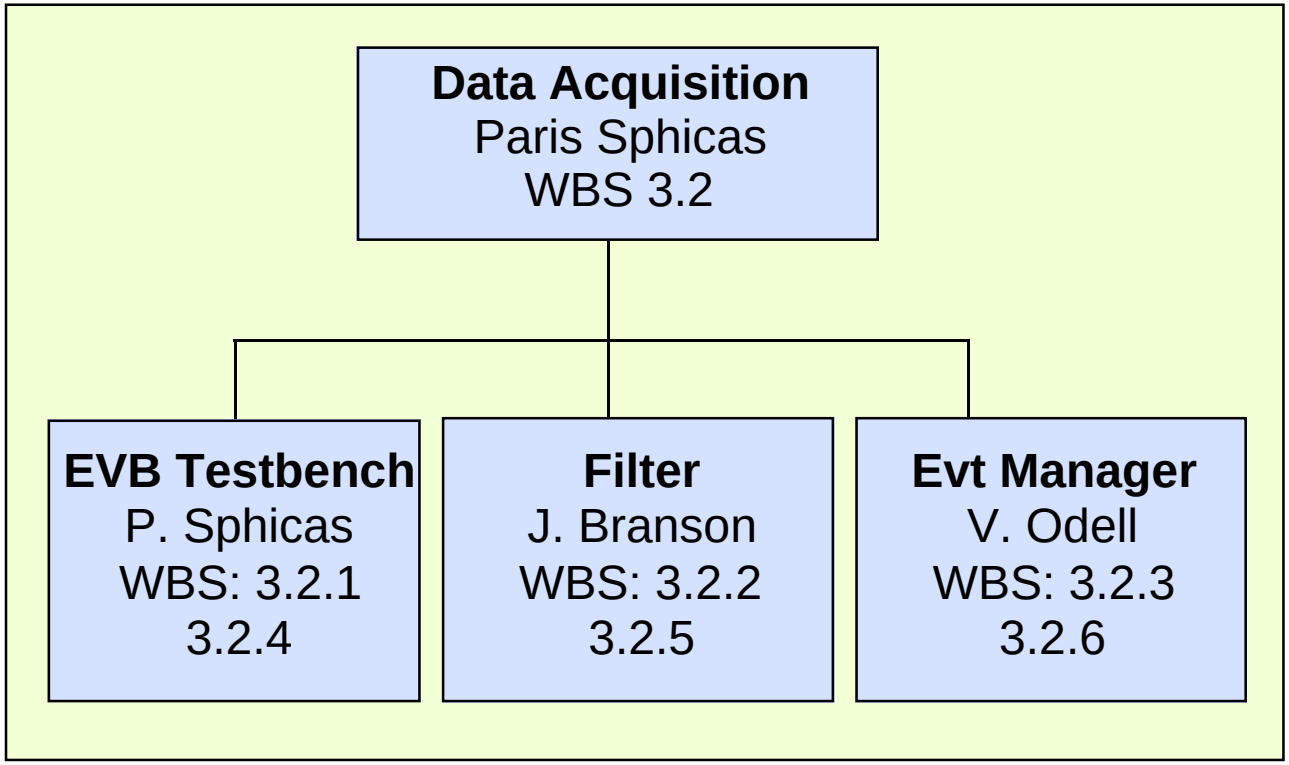
Organization

Organization: CMS DAQ
Organization: US_CMS DAQ
DAQ Project Management

Organization: CMS DAQ



Organization: US_CMS DAQ



Logic:

- **Same L3 manager for R&D and production**
  e.g.: V. Odell for Event Manager development (3.2.3) and production (3.2.6)

DAQ Project Management

CMS Annual Reviews

- **April: TriDAS Status**
  - Progress, draft R&D plans & expenses for next year
- **November: TriDAS Internal Review**
  - R&D Plans/Progress, Cost & Schedule
  - Internal detailed CMS Review of work so far + plan

US Reviews/Reporting

- **Report on CMS weeks (every three months)**
  - Review progress, expenditures, plan next 3 months
- **Meetings at FNAL and CERN (every ~ 6 weeks)**
  - EVM work with FNAL
  - FU work with MIT/UCSD (desktop/Vortex)
- **Currently being planned:**
  - Annual site visits

Milestones/Schedule

Phases/Milestones
MS Project Schedule

Phases/Milestones

1996-2001 Technical design

- Identify functions and subsystems by prototyping
- Select technologies and options by integration of test benches (lab) and demonstrators in test beams

2001-2002 Demonstrator

- 32x32 Event Builder; full DAQ prototype in testbeam

2002-2004 Construction/Procurement

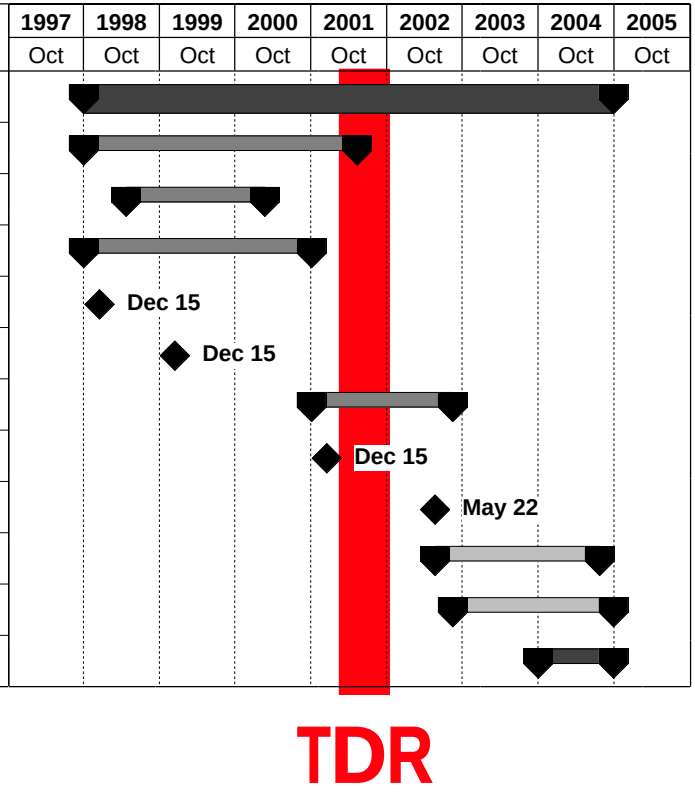
- System engineering, production, tests, purchasing, installation and detector subsystems integration.
- On-line software development. Documentation.

2005-2028 Operation

- Start data taking.

MS Project Schedule

ID	WBS	Task Name	Duration
1	3.2	**Data Acquisition**	1746.2d
2	3.2.1	**Prototypes: RU**	900d
38	3.2.2	**Prototypes: FU**	456d
53	3.2.3	**Prototypes: Event Build**	751d
80	3.2.0.1	Internal Design Review 1	0d
81	3.2.0.2	Internal Design Review 2	0d
82	3.2.4	**Demonstrator at Testbea**	465d
140	3.2.0.3	Internal Design Review 3	0d
141	3.2.0.4	Final Design Review	0d
142	3.2.5	**Production: Filter Unit**	543.75d
213	3.2.6	**Production: Event Build**	530.2d
221	3.2.7	**DAQ Tests/Installation**	245d



Evolution of US-DAQ project

Status at Lehman-I
Old (1997) US responsibility
Towards Lehman-II
DAQ Descoping
New US responsibility (I)
US DAQ project summary

Status at Lehman-I

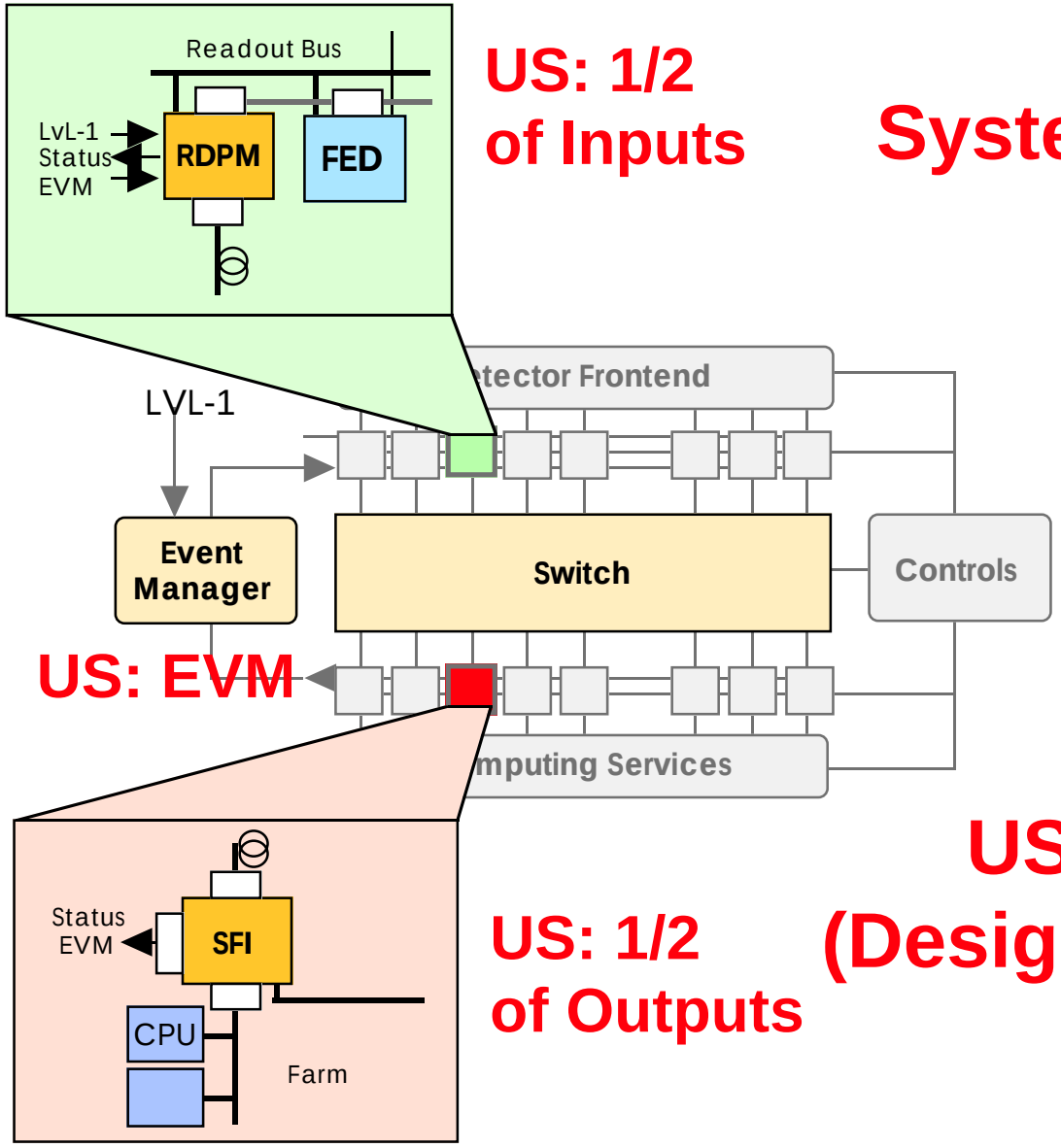
US-CERN collaboration:

- **From the beginning:**
  equal partnership, as long as equal "contributions"
- **Costs were confined to development:**
  - exclude switch
  - exclude farm
  - include: Inputs, Outputs, EVM

Agreement:

- **CERN and US work on <u>both inputs & outputs</u>**
- **US designs & builds Event Manager**
- **CERN and CH picks up switch**
- **CERN does most of farm (+FR+deficit)**
- **US: main development institutions:**
  FNAL, MIT, UCSD

Old (1997) US responsibility



US: 1/2 of Inputs

US: EVM

US: 1/2 of Outputs

System = Total
– Switch
– Farm
= Inputs
+ Outputs
+ EVM

US_CMS=0.5 (Design+Production)

Towards Lehman-II

US DAQ Project parameters at Lehman-I:

- Schedule (and thus funding profile) peaked late
- WBS: 3.2.1 to 3.2.10
- 5 development and 3 construction projects
- Costs:

M & S	5.1 M$	
EDIA	1.6 M$	
Contng	2.5 M$	(38%)

- TOTAL: 9.2 M$ (of which DOE 85%)

New facts:

- New contingency rules imply higher DAQ TEC
- Ditto for Level-1 Trigger
- CMS-wide descope scenarios

DAQ Descoping

Analysis of Situation:

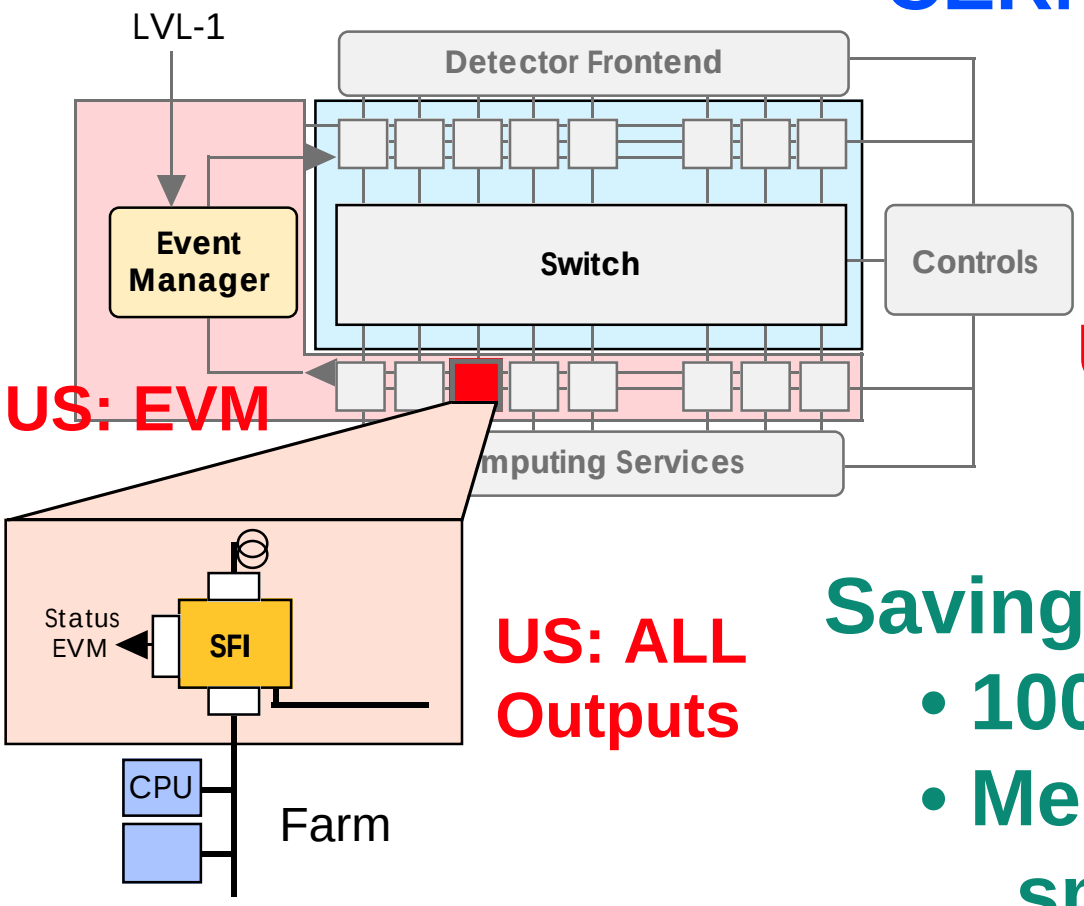
- **Keeping the same US responsibilities, but applying new contingency rules, would bring the total DAQ (US) cost to 10.6 M$**
- **Recall, cost at Lehman-I was 9.2 M$**
- **Similarly, Level-1 Trigger increase**
- **The above were recognized very early in this process, so we concentrated our efforts on:**
  (a) a change in US responsibility and
  (b) a redesign

Solution:

- **CMS-wide: DAQ scaled from 100 kHz to 75 kHz**
- **US-specific: Consolidate baseline; US is now**
  - ALL outputs and EVM

New US responsibility (I)

CERN = Inputs + Switch



US: EVM

US = Outputs + EVM

US: ALL Outputs

Savings:

- **100 kHz → 75 kHz**
- **Memory on output smaller (Level-2 rejection)**

US DAQ project summary

Result:

- Schedule (thus funding profile) still peaks late
- WBS: 3.2.1 to 3.2.7 (instead to 2.1.10)
- 2 construction projects (instead of 3)
- Costs:

M & S	3.5 M$	
EDIA	1.3 M$	
Contng	2.6 M$	(54%)

- TOTAL: 7.4 M$ (of which DOE 85%)

Remarks:

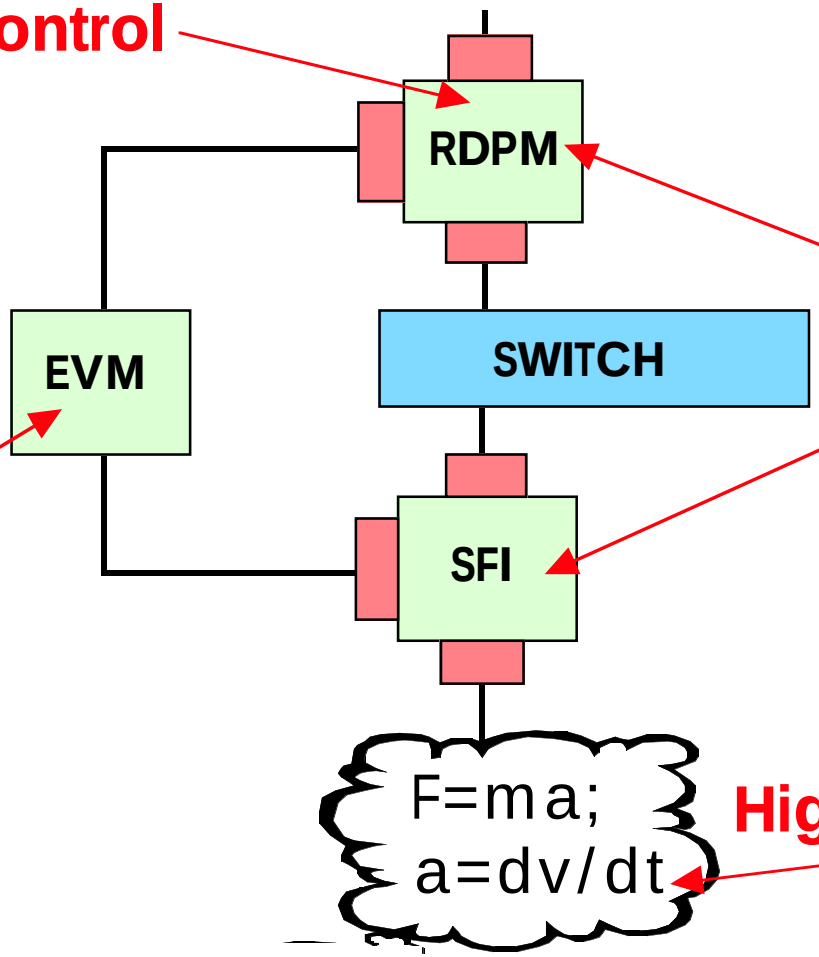
- System remains scalable (if unforeseen needs)
- Maintain partnership with CERN
- Full participation in system definition, design, and development

Status & Progress

S&P (I): R&D Tasks
S&P (II): Filter Unit
S&P (III): Event Manager
S&P (IV): Event Builder Testbench
S&P (V): Simulation

S&P (I): R&D Tasks

Readout Control
UCLA



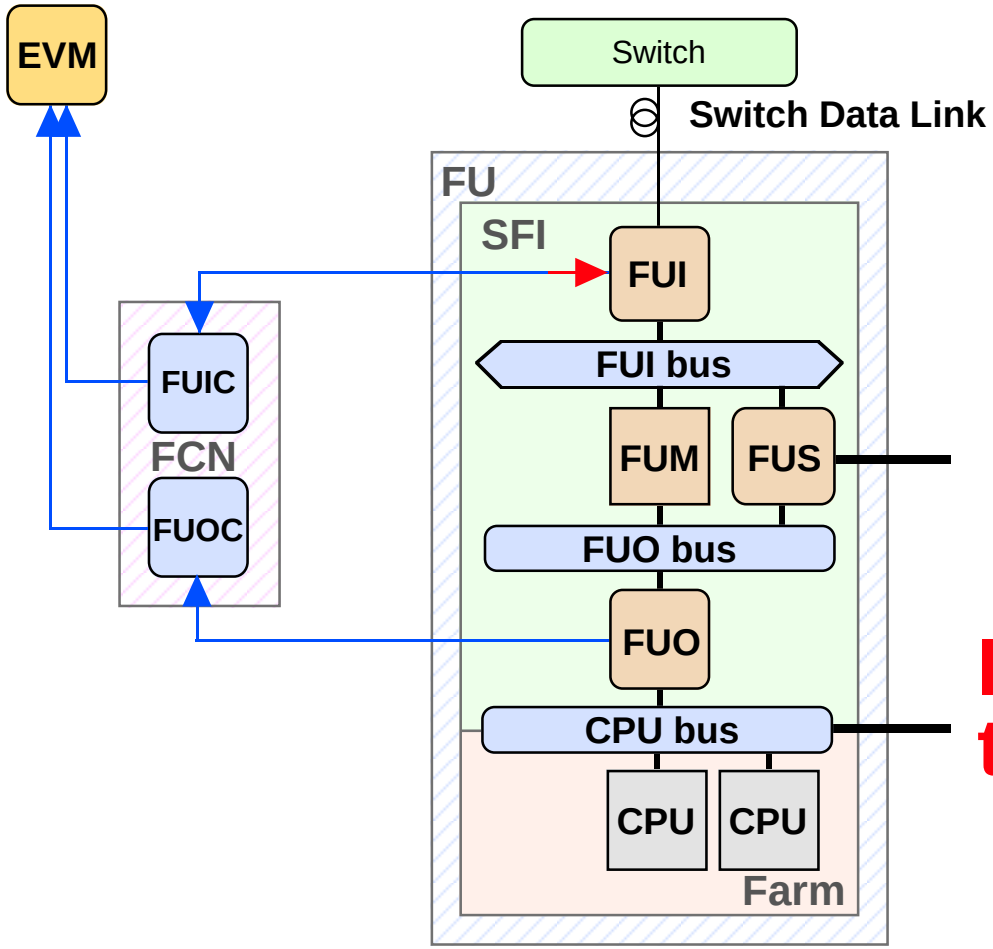
Dual Port Memories (DPM)
UCSD, MIT (+CERN)

EVM
FNAL, MIT

High Level Triggers
ALL

Simulation of protocols, system parameters
MIT

S&P (II): Filter Unit



EVM	**Event Manager**
DSN	DAQ Services Network
FCN	Farm Control Network
FUIC	FU Input Controller
FUOC	FU Output Controller
CSN	Computing&Services Network

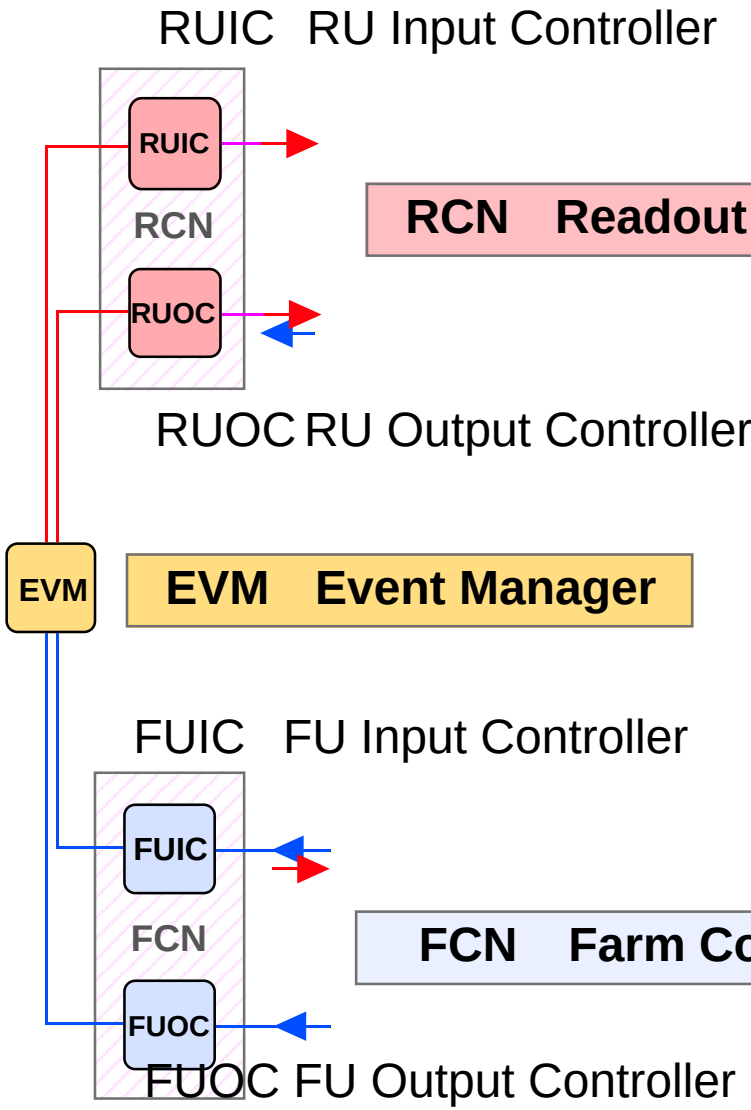
FU	**Filter Unit**
FUI	Filter Unit Input
FUM	Filter Unit Memory
FUO	Filter Unit Output
FUS	FU Supervisor

Investigating two solutions:

(a) desktop-like intelligence (e.g. PC)

(b) special module does FUI+FUM+FUS

S&P (III): Event Manager



Currently:

(a) Reflective-memory type network (CDF)
(b) Ethernet with switches (near future?)

S&P (IV): Event Builder Testbench

Using CDF upgrade as CMS prototype

- Joint R&D between CDF II, FNAL CD, US_CMS
- Same for Level-3 processor farm → Filter Unit
- Data from testbench → check simulation
- Lots of results obtained
- ATM-based event builder reviewed by CDF, approved for completion by mid-99.

Installation in CDF "Level-3" counting room

S&P (V): Simulation

Very large effort dedicated to simulation

- C++ based for full system; functional level
- VHDL for individual components
- Foresight for module descriptions

- **Many results; examples:**

Destination assignment

Simple cyclic

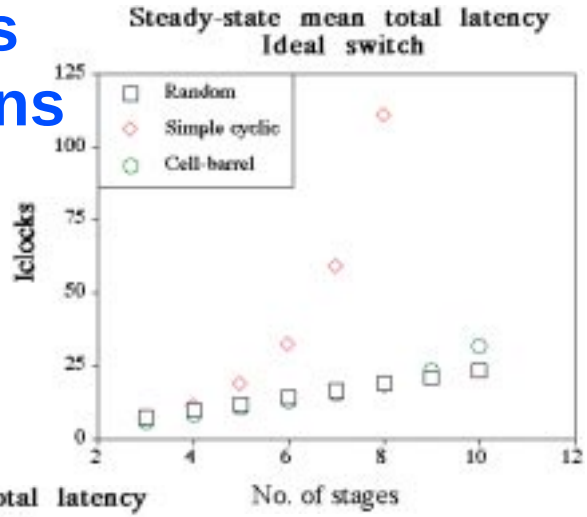
0	3	2	1	0	→ Source 0
0	3	2	1	0	→ Source 1
0	3	2	1	0	→ Source 2
0	3	2	1	0	→ Source 3

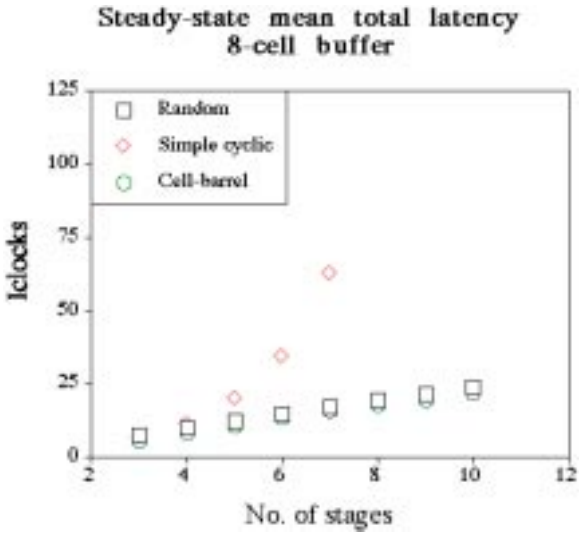
Cell-based barrel shifter

0	3	2	1	0	→ Source 0
1	0	3	2	1	→ Source 1
2	1	0	3	2	→ Source 2
3	2	1	0	3	→ Source 3

Random

3	0	2	3	3	→ Source 0
3	2	1	3	0	→ Source 1
2	0	2	0	3	→ Source 2
2	1	1	0	0	→ Source 3





WBS Summary

WBS: costing methodology
WBS: technology evolution
WBS: summary
WBS: cost drivers
Contingency

WBS: costing methodology

Two strategies:

1. Take high-end, apply deflation
2. Take today's "standard" product, apply same price, but assume performance increase

We adopted strategy 2:

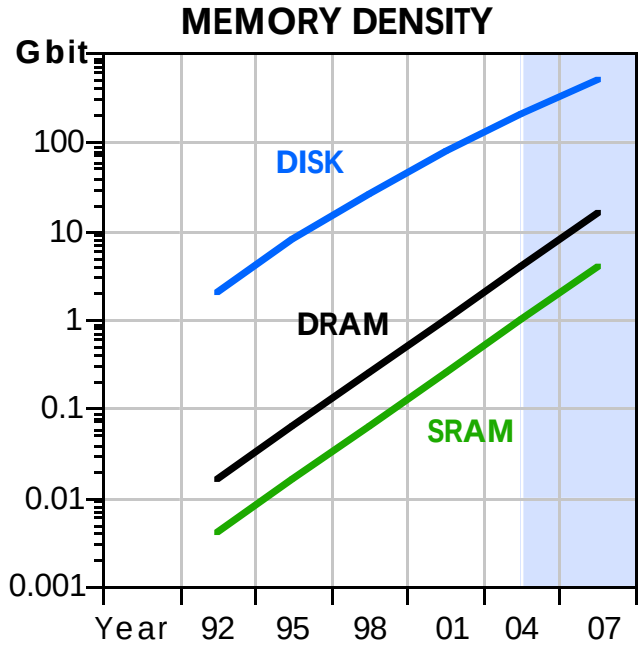
- Commercial PC's cost the same (3,000$) each Xmas buying season: MHz, MB and GB go up
- Easier to extrapolate performance
- More examples to back up strategy

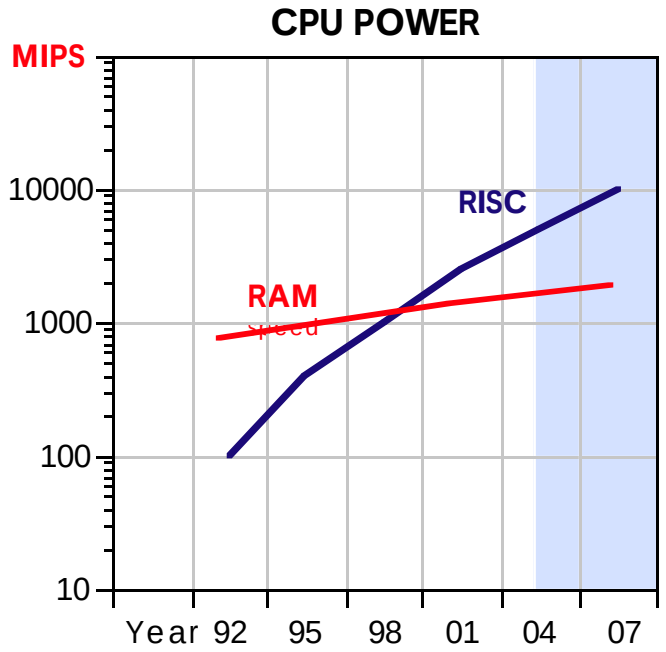
Examples of strategy 2:

- Memory chip density evolution
- CPU frequency evolution
- Switch interfaces speed evolution

Full details/examples in parallel session

WBS: technology evolution



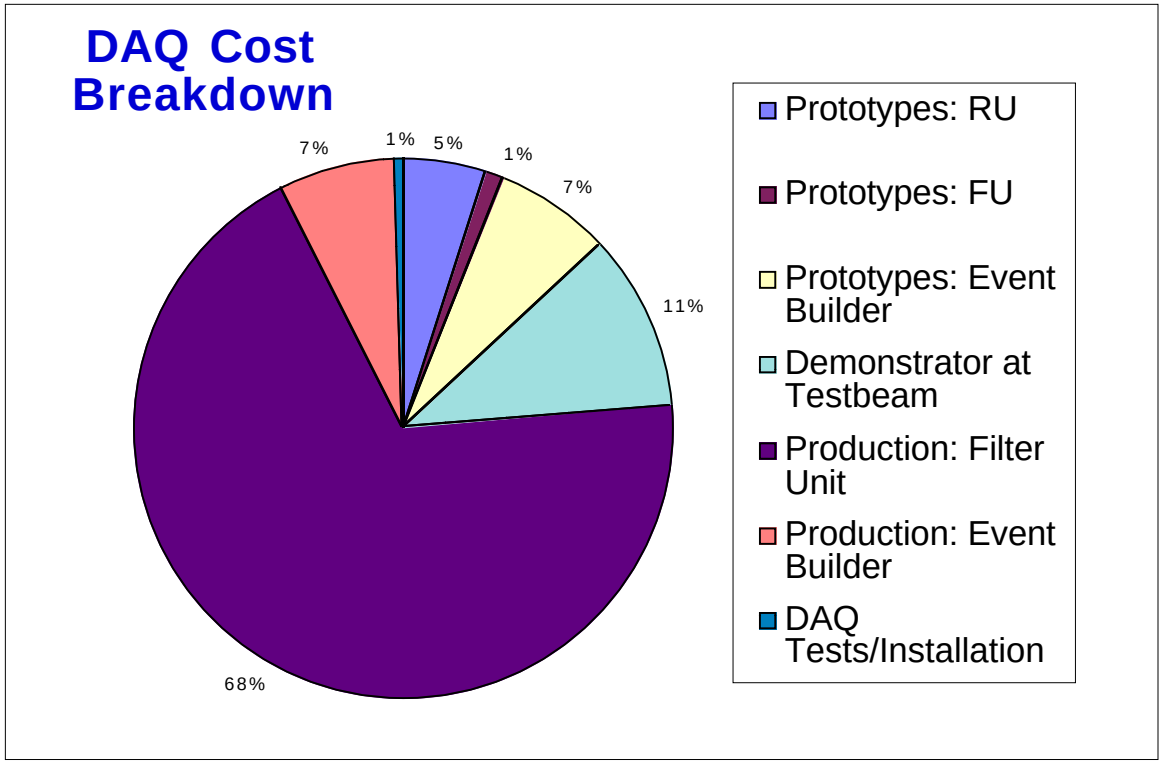


- The CPU processing power increases by a factor 10 every 5 years
- Memory density increases by a factor 4 every two years
- The 90's is the data communication decade

WBS: summary

Total Cost: 4.8 M$

- M&S 3.5 M$
- EDIA 1.3 M$

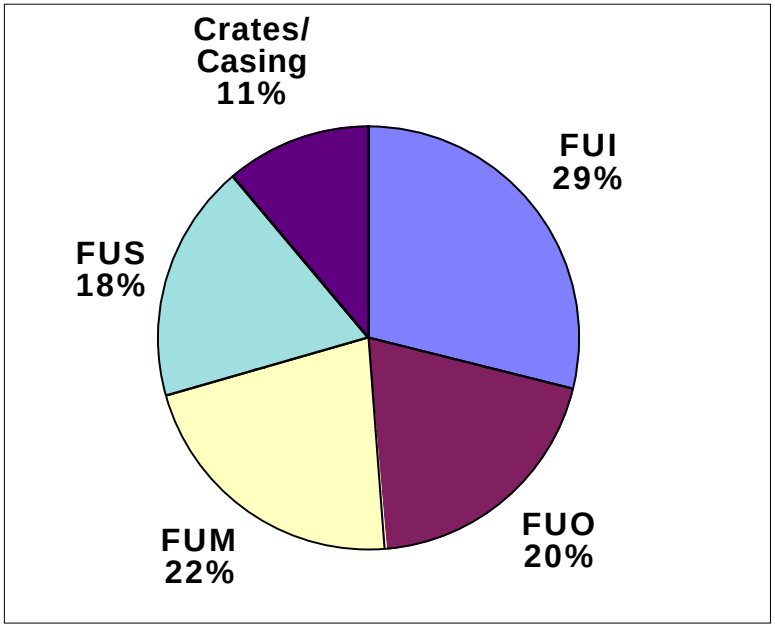


Contingency:

2.6 M$ (54 % of total cost)

- Applied at deepest level of WBS

WBS: cost drivers



Main costs:

- **Production of Filter Units**

Basis of estimate:

- **M&S:**

  For each functional unit (e.g. FUI) find commercial component that has factor 4-5 less performance than requirements, apply today's costs.

- **EDIA:**

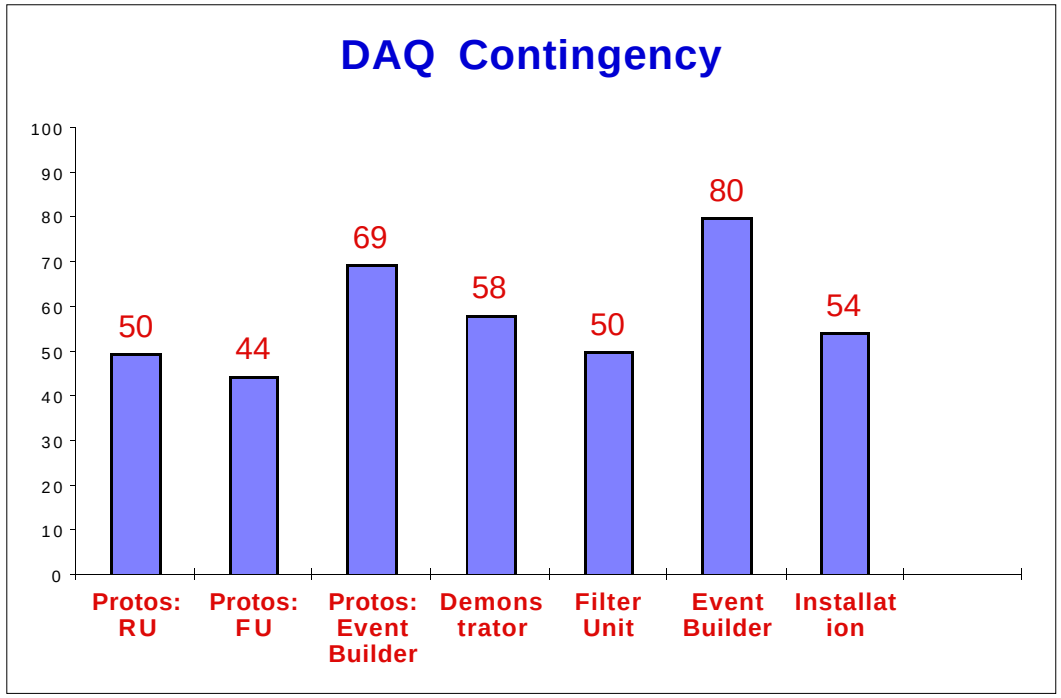
  CMS R&D so far (protos) + CDF upgrade

Contingency

Used standard US_CMS definitions

- Contingency = DM*JF
- Design Maturiry: 1.3-1.5; Judgement Factor: 1.0-1.2

Contingency was determined and applied at deepest WBS level



Resulting project contingency: 54%

Commitment and Resource Profiles

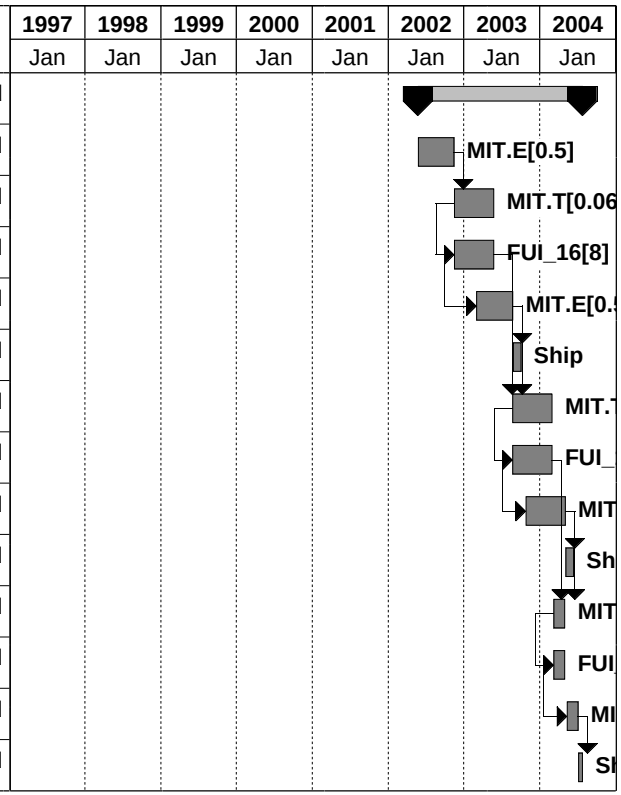
Schedule (MS Project) + profiles
Manpower Profile
Obligations Profile

Schedule (MS Project) + profiles

Resource-loaded schedule; example from prod

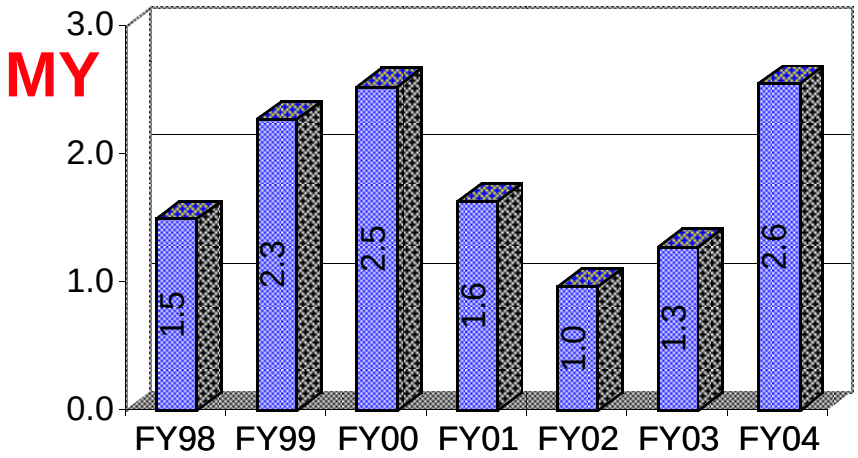
- Final blueprint → Order 1 → Order 1 Test → Shipping → Order 2...

ID	WBS	Task Name	Duration
143	**3.2.5.1**	**FUI**	**543.75d**
144	3.2.5.1.1	Final FUI blueprir	125d
145	3.2.5.1.2	FUI Order 1 mana	125d
146	3.2.5.1.3	FUI Order 1	125d
147	3.2.5.1.4	FUI Batch 1 Test	125d
148	3.2.5.1.5	FUI Batch 1 Shipı	30d
149	3.2.5.1.6	FUI Order 2 mana	125d
150	3.2.5.1.7	FUI Order 2	125d
151	3.2.5.1.8	FUI Batch 2 Test	125d
152	3.2.5.1.9	FUI Order 2 Shipı	30d
153	3.2.5.1.10	FUI Spares mana	40d
154	3.2.5.1.11	FUI Spares	40d
155	3.2.5.1.12	FUI Spares Test	40d
156	3.2.5.1.13	FUI Spares Shipr	15d



Manpower Profile

Software

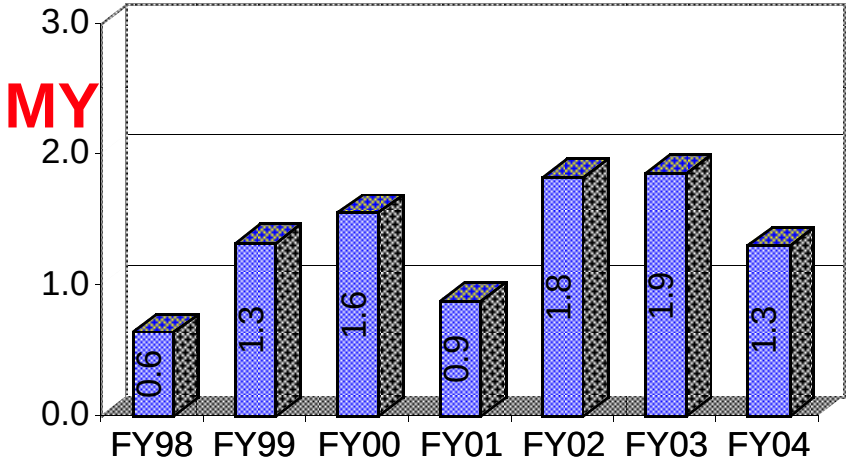


R&D

Demo

Prod

Engineers

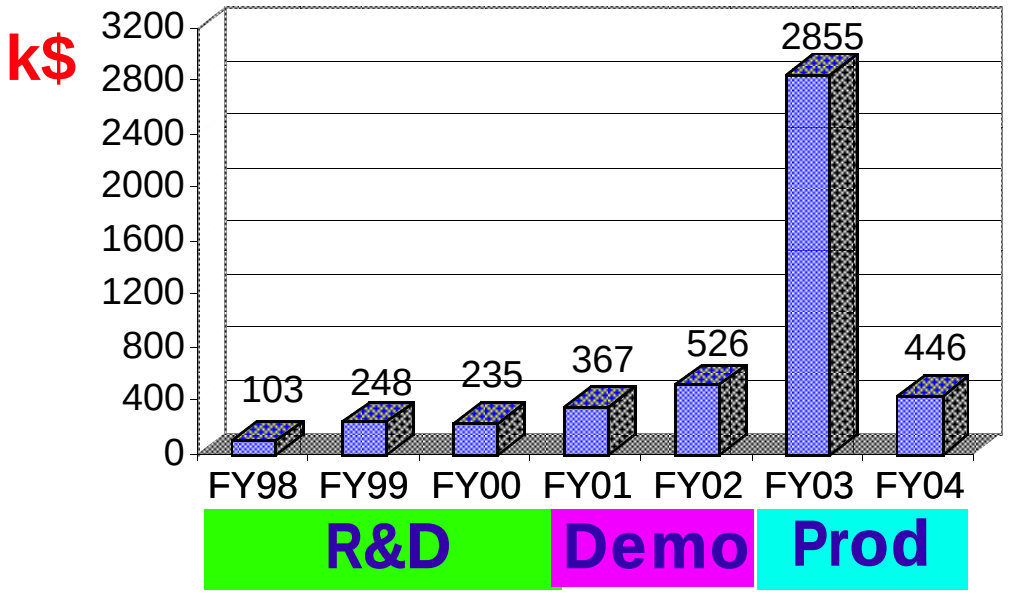


R&D

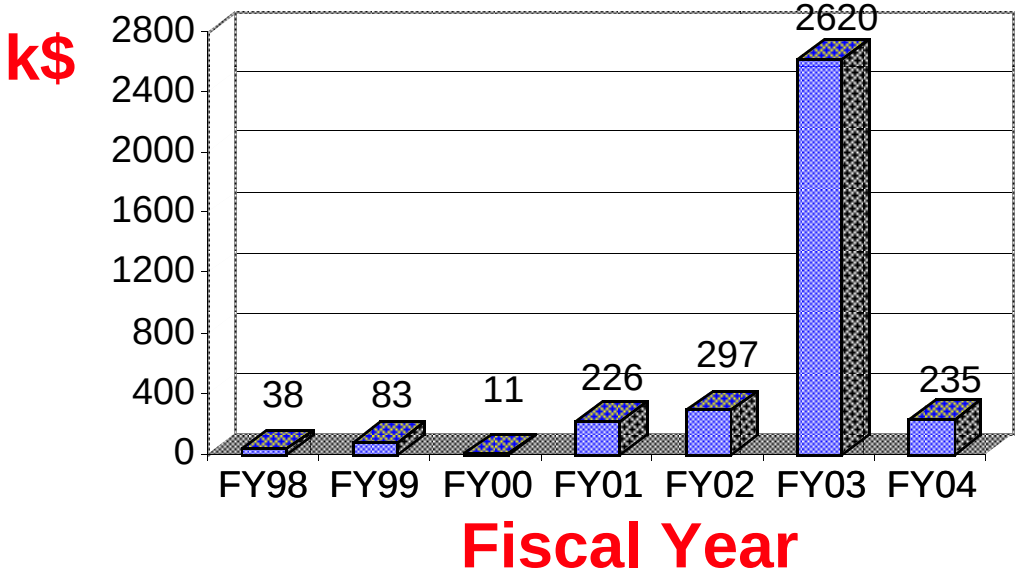
Demo

Prod

Obligations Profile



Total



M&S

Concerns & Actions taken

Comments from Lehman-I
Simulation: 8x8 blocks
8x8: Results

Comments from Lehman-I

- **Base ... contingency and risk on the maturity of the design, and specify it item by item, rather than globally...**

DONE. Contingency applied at deepest WBS level

- **Give more attention and effort to integrating the simulation of the overall DAQ ... in order to verify the assumptions about the total system performance.**

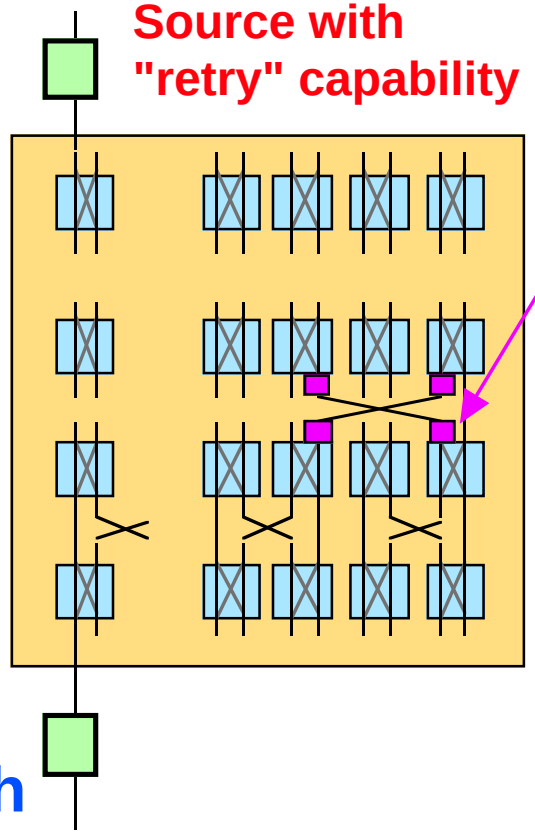
On-going effort, to be completed by TDR (2001). Numerous results obtained confirming current parameters.

- **Develop the backup plan for using multiple 32 x 32 switches in case the 512 x 512 switch is unobtainable.**

On-going effort. Identified one technology that is applicable TODAY already. Others under investigation.

Simulation: 8x8 blocks

- **What if a 512 x 512 switch is not available?**
- **Multistage-multiswitch solution, for example collection of 32 x 32 switches appropriately interconnected.**



Memory between basic switching unit → absorb collisions

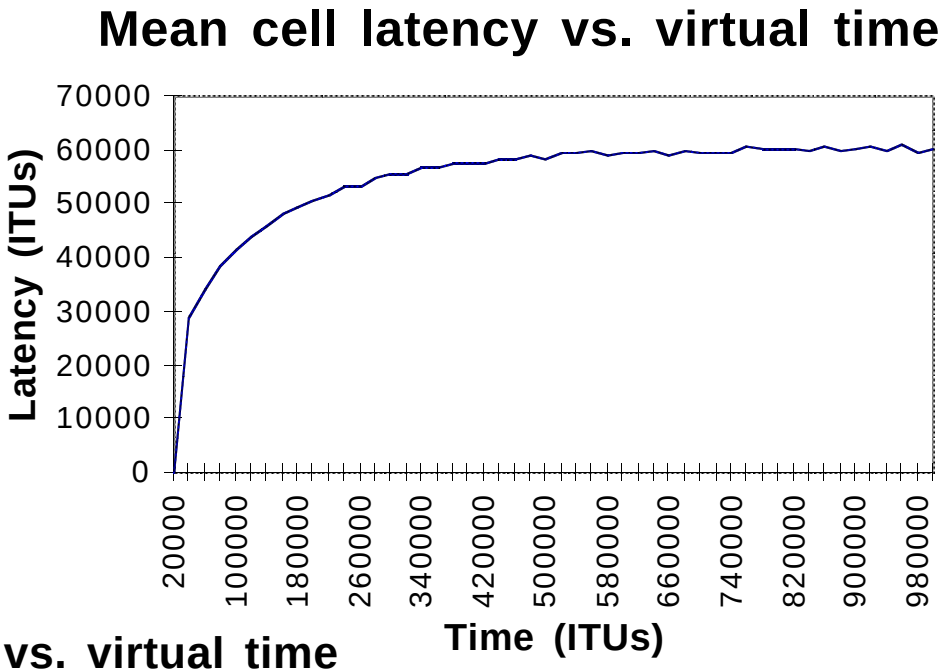
→ must have "retry" capability...
Issues: how much memory in between switching elements?
Adequacy of commercial systems an issue...

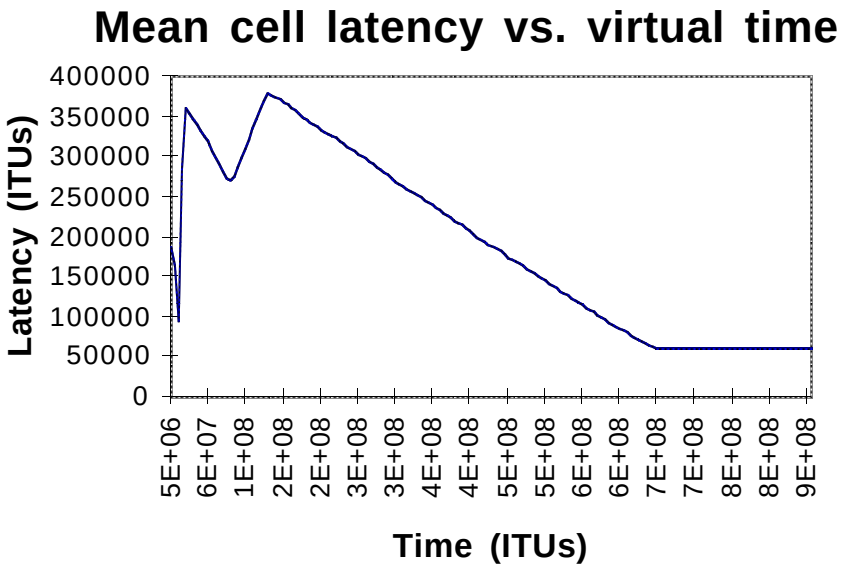
- **Currently under investigation:**

(a) with simulation
(b) in FY98: with appropriately connecting switch outputs into switch inputs with and without intermediate memory.

8x8: Results

EVB: 512x512 made out of 8x8 switches





EVB: effect of a data "shock"

Summary & Conclusion

CMS DAQ descoped: 100 kHz → 75 kHz

US_CMS responsibility on DAQ consolidated:

- **ALL switch outputs + Event Manager**

Costs:	**Old**	**New**	
Total	**6.8 M$**	**4.8 M$**	
Cont	**38%**	**54%**	
TEC	**9.2 M$**	**7.4 M$**	**(–20%)**

(and contingency applied at deepest WBS level)

Progress since last review:

(a) Technical: New (more modular) design for DAQ; Much more simulation; Event Builder Testbench → results

(b) Costing: consolidated; based on today's commercially available items + assume factor ~4 increase in performance